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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/651,458	YAMAZAKI ET AL.
	Examiner	Art Unit
	Thao X. Le	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/517,542.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: numeral 317 and 334 in fig. 11. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance. Furthermore, 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms". The Applicant is requested reviewing the disclosure carefully for any errors.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 42-77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Recite the limitation "organic EL layer" in claims 42, 47, 52, 57, 62, 67, there is insufficient antecedent basis for this limitation in the claim.

Assuming the limitation would read as "EL layer" for the purpose of examination.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 42-45, 47-49, 51, and 72-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6518962 to Kimura et al. in view of US 4839707 to Shields and US 6831623 to Yasukawa.

Regarding claim 42, Kimura discloses a display device in fig. 20 comprising: a glass substrate 1, col. 17 line 19, column 37 line 11, a switching transistor 221, column 20 line 27, and a current controlling transistor 223, column 20 line 28, formed on the substrate each comprising a source region a drain region, see claim 2, and a gate electrode 131, column 37 line 18, and a gate insulating film 251, column 37 line 18, an interlayer insulating film 252 formed over the switching transistor 221 and the controlling transistor 223, an electrode 132 electrically connected with one of the source region and the drain region of the switching transistor 221, and formed over the interlayer insulating film 252, a dielectric layer 253 formed on the electrode 132, a power supply line 133, column 20 line 53, electrically connected with one of the source region and the drain region of the current controlling transistors 223, a first electrode 141, column 37 line 25, electrically connected with the other one of the source region and the drain region of the current controlling transistors 223, an EL layer 224, column 37 line 17, formed over the first electrode 141; and a second electrode 105, column 37 line 24, formed over the EL layer 224.

But, Kimura does not expressly disclose the device comprising an insulating layer formed on the semiconductor substrate and a power supply line formed on the dielectric layer.

However, Shields discloses a display device in fig. 1 comprising a semiconductor layer 15, column 4 line 18, formed on an upper surface of the insulating layer 13 column 4 line 18, and a gate electrode 29, column 45 line 34, adjacent to the semiconductor layer 15 with a gate insulating 27, column 4 line 34, interposed therebetween (SOI substrate). At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the SOI teaching of Shields with display device of Kimura, because the SOI structure would have isolated both the polysilicon layer and the device layer that would have eliminated shorts rising from leaky diodes as taught by Shields, column 3 line 55-60. Furthermore, a TFT transistor can be formed in different type substrates such as glass or semiconductor are typical in the art, see Yamada (6781155) in col. 5 lines 57-59, Aoki (6307532) in col. 17 lines 8-10, Takayama (5677549) in col. 1 line 15), or Kusumoto (5612565) in col. 4 line 10-12.

With respect to 'power supply formed on the dielectric layer', Yasukawa discloses a display device in fig. 2-3, 5 and 6 comprises a switching transistor (with gate 4a), fig. 2, a controlling transistor (with gate 4a'), an interlayer insulating layer 6 formed over the transistors, an electrode 27a electrically connected to the S/D 5a/b of the switching transistor and formed over the interlayer insulating film 6, fig. 2, a dielectric layer 11 formed on the electrode 27a, a power supply line electrically connected with one of the S/D 5a' of the controlling transistor, and formed on the dielectric layer 6, a first electrode 27c electrically connected with the other one S/G region 5b'of the controlling

transistor, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrode connection teaching of Yasukawa with Kimura's device because it would have reduced the light leakage current or the light leaking into the pixel region and peripheral circuits as taught by Yasukawa in col. 2 lines 26-30.

Regarding claims 43, 51, Kimura discloses a display device wherein the display device is incorporated in at least one selected from the group consisting of a portable telephone, a video camera, a mobile computer, a goggle type display, a projector, an electronic book, a digital camera, and a DVD player, fig. 24-25 column 40 lines 35-55.

Regarding claims 44, 48, Kimura discloses the display device according to claim 42, wherein the first electrode 141 overlaps the power supply line 133 (extending portion of 133 to FET 110), fig. 1 and 20.

Regarding claims 45, 49, Kimura discloses the display device, wherein the electrode (right portion next to 131) comprises one selected from the group consisting of Al, Ta and Ti, column 37 line 20.

Regarding claim 47, Kimura discloses a display device in fig. 20 comprising: a glass substrate 1, col. 17 line 19, col. 37 line 11, a p-channel switching transistor 221, column 20 line 27 and column 39 line 52, and a n-channel current controlling transistor 223, column 20 line 28 and column 30 line 25, formed on the substrate each comprising a source region a drain region, see claim 2, and a gate electrode 131, column 37 line 18, and a gate insulating film 251, an interlayer insulating film 252 formed over the p-channel type switching transistor and the n-channel type current controlling transistor,

an electrode 132 electrically connected with one of the source region and the drain region of the p-channel switching transistor 221, and formed over the interlayer insulating film 252, a dielectric layer 253 formed on the electrode 132, a power supply line 133, column 20 line 53, electrically connected with one of the source region and the drain region of the n-channel current controlling transistors 223, a first electrode 141, column 37 line 25, electrically connected with the other one of the source region and the drain region of the current controlling transistors 223, an EL layer 224, column 37 line 17, formed over the first electrode 141; and a second electrode 105, column 37 line 24, formed over the EL layer 224.

But, Kimura does not expressly disclose the device comprising an insulating layer formed on the semiconductor substrate, and a power supply line formed on the dielectric layer.

However, Shields discloses a display device in fig. 1 comprising a semiconductor layer 15, column 4 line 18, formed on an upper surface of the insulating layer 13 column 4 line 18, and a gate electrode 29, column 45 line 34, adjacent to the semiconductor layer 15 with a gate insulating 27, column 4 line 34, interposed therebetween (SOI substrate). At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the SOI teaching of Shields with display device of Kimura, because the SOI structure would have isolated both the polysilicon layer and the device layer that would have eliminated shorts rising from leaky diodes as taught by Shields, column 3 line 55-60. Furthermore, a TFT transistor can be formed in different type

substrates such as glass or semiconductor are typical in the art, see Yamada (6781155) in col. 5 lines 57-59, Aoki (6307532) in col. 17 lines 8-10, Takayama (5677549) in col. 1 line 15), or Kusumoto (5612565) in col. 4 line 10-12.

With respect to 'power supply formed on the dielectric layer', Yasukawa discloses a display device in fig. 2-3, 5 and 6 comprises a switching transistor (with gate 4a), fig. 2, a controlling transistor (with gate 4a'), an interlayer insulating layer 6 formed over the transistors, an electrode 27a electrically connected to the S/D 5a/b of the switching transistor and formed over the interlayer insulating film 6, fig. 2, a dielectric layer 11 formed on the electrode 27a, a power supply line electrically connected with one of the S/D 5a' of the controlling transistor, and formed on the dielectric layer 6, a first electrode 27c electrically connected with the other one S/G region 5b'of the controlling transistor, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrode connection teaching of Yasukawa with Kimura's device because it would have reduced the light leakage current or the light leaking into the pixel region and peripheral circuits as taught by Yasukawa in col. 2 lines 26-30.

Regarding claim 72-72, Kimura discloses the display device wherein the EL layer 224 is organic, col. 20 line 37.

7. Claims 52-54, 57-59, 61-69, 71, 74-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6518962 to Kimura et al. in view of US 6831623 to Yasukawa.

Regarding claims 52, Kimura discloses a display device in fig. 20 comprising: a glass substrate 1, col. 17 line 19, column 37 line 11, a switching transistor 221, column 20 line 27, and a current controlling transistor 223, column 20 line 28, formed on the substrate each comprising a source region a drain region, see claim 2, and a gate electrode 131, column 37 line 18, and a gate insulating film 251, column 37 line 18, an interlayer insulating film 252 formed over the switching transistor and the current controlling transistor, an electrode 132 electrically connected with one of the source region and the drain region of the switching transistor 221, and formed over the interlayer insulating film 252, a dielectric layer 253 formed on the electrode 132, a power supply line 133, column 20 line 53, electrically connected with one of the source region and the drain region of the current controlling transistors 223, fig. 20, a first electrode 141, column 37 line 25, electrically connected with the other one of the source region and the drain region of the current controlling transistors 223, an organic EL layer 224, column 37 line 17, formed over the first electrode 141; and a second electrode 105, column 37 line 24, formed over the organic EL layer 224.

But Kimura does not disclose a semiconductor substrate and a power supply line formed on the dielectric layer.

However, Yasukawa discloses a display device in fig. 2-3, 5 and 6 comprises a semiconductor substrate 1, a switching transistor (with gate 4a), fig. 2, a controlling transistor (with gate 4a'), an interlayer insulating layer 6 formed over the transistors, an electrode 27a electrically connected to the S/D 5a/b of the switching transistor and formed over the interlayer insulating film 6, fig. 2, a

dielectric layer 11 formed on the electrode 27a, a power supply line electrically connected with one of the S/D 5a' of the controlling transistor, and formed on the dielectric layer 6, a first electrode 27c electrically connected with the other one S/G region 5b'of the controlling transistor, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrode connection teaching of Yasukawa with Kimura's device because it would have reduced the light leakage current or the light leaking into the pixel region and peripheral circuits as taught by Yasukawa in col. 2 lines 26-30.

Regarding claims 53, 58, 63, and 68, Kimura discloses the display device wherein the first electrode 141 overlaps the power supply line 133 (extending portion of 133 to FET 110), fig. 1 and 20.

Regarding claims 54, 59, 64, and 69, Kimura discloses the display device wherein the electrode (right portion of 131) comprises one selected from the group consisting of Al, Ta and Ti, column 37 line 20.

Regarding claims 61 65-66, and 71, Kimura discloses a display device wherein the display device is incorporated in at least one selected from the group consisting of a portable telephone, a video camera, a mobile computer, a goggle type display, a projector, an electronic book, a digital camera, and a DVD player, fig. 24-25 column 40 lines 35-55.

Regarding claim 57, Kimura discloses a display device in fig. 20 comprising: a glass substrate 1, col. 17 line 19, column 37 line 11, a p-channel switching transistor 221, column 20 line 27 and column 39 line 52, and a n-channel current controlling

transistor 223, column 20 line 28 and column 30 line 25, formed on the substrate each comprising a source region a drain region, see claim 2, and a gate electrode 131, column 37 line 18, and a gate insulating film 251, an interlayer insulating film 252 formed over the p-channel type switching transistor and the n-channel type current controlling transistor, an electrode 132 electrically connected with one of the source region and the drain region of the p-channel switching transistor 221, a dielectric layer 253 formed on the electrode 132, a power supply line 133, column 20 line 53, electrically connected with one of the source region and the drain region of the n-channel current controlling transistors 223, fig. 20, a first electrode 141, column 37 line 25, electrically connected with the other one of the source region and the drain region of the n-channel type current controlling transistors 223, fig. 20, an EL layer 224, column 37 line 17, formed over the first electrode 141; and a second electrode 105, column 37 line 24, formed over the EL layer 224.

But Kimura does not disclose a semiconductor substrate and a power supply line formed on the dielectric layer.

However, Yasukawa discloses a display device in fig. 2-3, 5 and 6 comprises a semiconductor substrate 1, a switching transistor (with gate 4a), fig. 2, a controlling transistor (with gate 4a'), an interlayer insulating layer 6 formed over the transistors, an electrode 27a electrically connected to the S/D 5a/b of the switching transistor and formed over the interlayer insulating film 6, fig. 2, a dielectric layer 11 formed on the electrode 27a, a power supply line electrically connected with one of the S/D 5a' of the controlling transistor, and formed on the

dielectric layer 6, a first electrode 27c electrically connected with the other one S/G region 5b'of the controlling transistor, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrode connection teaching of Yasukawa with Kimura's device because it would have reduced the light leakage current or the light leaking into the pixel region and peripheral circuits as taught by Yasukawa in col. 2 lines 26-30.

Regarding claims 62, Kimura discloses a display device in fig. 20 comprising: a glass substrate 1, col. 17 line 19, column 37 line 11, a switching transistor 221, column 20 line 27, and a current controlling transistor 223, column 20 line 28, formed on the substrate each comprising a source region a drain region, see claim 2, and a gate electrode 131, column 37 line 18, and a gate insulating film 251, column 37 line 18, an interlayer insulating film 252 formed over the switching transistor and the current controlling transistor, an electrode 132 electrically connected with one of the source region and the drain region of the switching transistor 221, and formed over the interlayer insulating film 252, a dielectric layer 253 formed on the electrode 132, a power supply line 133, column 20 line 53, electrically connected with one of the source region and the drain region of the current controlling transistors 223, storage capacitor comprising the electrode 132, the dielectric layer 253, and the power supply line 133, fig. 20, a first electrode 141, column 37 line 25, electrically connected with the other one of the source region and the drain region of the current controlling transistors 223, an EL layer 224, column 37 line 17, formed over the first electrode 141; and a second electrode 105, column 37 line 24, formed over the EL layer 224.

But Kimura does not disclose a semiconductor substrate and a power supply line formed on the dielectric layer.

However, Yasukawa discloses a display device in fig. 2-3, 5 and 6 comprises a semiconductor substrate 1, a switching transistor (with gate 4a), fig. 2, a controlling transistor (with gate 4a'), an interlayer insulating layer 6 formed over the transistors, an electrode 27a electrically connected to the S/D 5a/b of the switching transistor and formed over the interlayer insulating film 6, fig. 2, a dielectric layer 11 formed on the electrode 27a, a power supply line electrically connected with one of the S/D 5a' of the controlling transistor, and formed on the dielectric layer 6, a first electrode 27c electrically connected with the other one S/G region 5b'of the controlling transistor, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrode connection teaching of Yasukawa with Kimura's device because it would have reduced the light leakage current or the light leaking into the pixel region and peripheral circuits as taught by Yasukawa in col. 2 lines 26-30.

With respect to storage capacitor, Kimura or Yasukawa obviously discloses a capacitor that normally comprises a two electrodes and a dielectric layer interposes between two electrodes.

Regarding claim 67, Kimura discloses a display device in fig. 20 comprising: a glass substrate 1, col. 17 line 19, column 37 line 11, a p-channel switching transistor 221, column 20 line 27 and column 39 line 52, and a n-channel current controlling transistor 223, column 20 line 28 and column 30 line 25, formed on the substrate each

comprising a source region a drain region, see claim 2, and a gate electrode 131, column 37 line 18, and a gate insulating film 251, an interlayer insulating film 252 formed over the switching transistor and the current controlling transistor, an electrode 132 electrically connected with one of the source region and the drain region of the p-channel switching transistor 221, and formed over the interlayer insulating film 252, a dielectric layer 253 formed on the electrode 132, a power supply line 133, column 20 line 53, electrically connected with one of the source region and the drain region of the n-channel current controlling transistors 223, a storage capacitor comprising the electrode 132, the dielectric layer 253, and the power supply line 133, fig. 20, a first electrode 141, column 37 line 25, electrically connected with the other one of the source region and the drain region of the n-channel type current controlling transistors 223, fig. 20, an EL layer 224, column 37 line 17, formed over the first electrode 141; and a second electrode 105, column 37 line 24, formed over the EL layer 224.

But Kimura does not disclose a semiconductor substrate and a power supply line formed on the dielectric layer.

However, Yasukawa discloses a display device in fig. 2-3, 5 and 6 comprises a semiconductor substrate 1, a switching transistor (with gate 4a), fig. 2, a controlling transistor (with gate 4a'), an interlayer insulating layer 6 formed over the transistors, an electrode 27a electrically connected to the S/D 5a/b of the switching transistor and formed over the interlayer insulating film 6, fig. 2, a dielectric layer 11 formed on the electrode 27a, a power supply line electrically connected with one of the S/D 5a' of the controlling transistor, and formed on the

dielectric layer 6, a first electrode 27c electrically connected with the other one S/G region 5b'of the controlling transistor, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the electrode connection teaching of Yasukawa with Kimura's device because it would have reduced the light leakage current or the light leaking into the pixel region and peripheral circuits as taught by Yasukawa in col. 2 lines 26-30.

With respect to storage capacitor, Kimura or Yasukawa obviously discloses a capacitor that normally comprises a two electrodes and a dielectric layer interposes between two electrodes.

Regarding claim 72-72, Kimura discloses the display device wherein the EL layer 224 is organic, col. 20 line 37.

8. Claims 46, 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6518962 to Kimura et al. and US 4839707 to Shields and US 6831623 to Yasukawa as applied to the above claims 42 and 47 and further in view of US 5733661 to Ue et al.

Regarding claims 46, 50, Kimura does not disclose the display device wherein the electrode comprises oxidation film of the electrode.

However, Ue discloses a electrode 1, fig. 2, consists of Ta, Ti, or Ta, column 3 line 64, having a oxidation film 2, fig. 2, column 1 lines 19-22 or column 4 lines 1-5. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the aluminum electrode teaching of Shields and oxidation film of Ue with Kimura's device, because anodization would have created a metal oxide layer having high electrical insulation properties and

function to permits electric current to flow therethrough in one direction and can be used as a protective film for wiring in liquid crystal device as taught by Ue, column 1 lines 23-38, and column 4 line 10.

9. Claims 55, 60, 65, and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6518962 to Kimura et al. and US 6831623 to Yasukawa as applied to the above claims 52, 57, 62, and 67 and further in view of US 5733661 to Ue et al.

Regarding claims 55, 60, 65, and 71, Kimura does not disclose the display device wherein the dielectric comprises an oxidation film of the electrode.

However, Ue discloses a electrode 1, fig. 2, consists of Ta, Ti, or Ta, column 3 line 64, having a oxidation film 2, fig. 2, column 1 lines 19-22 or column 4 lines 1-5. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the aluminum electrode teaching of Shields and oxidation film of Ue with Kimura's device, because anodization would have created a metal oxide layer having high electrical insulation properties and function to permits electric current to flow therethrough in one direction and can be used as a protective film for wiring in liquid crystal device as taught by Ue, column 1 lines 23-38, and column 4 line 10.

Response to Arguments

10. Applicant's arguments with respect to claims 42-71 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
03 March 2006